AK4358

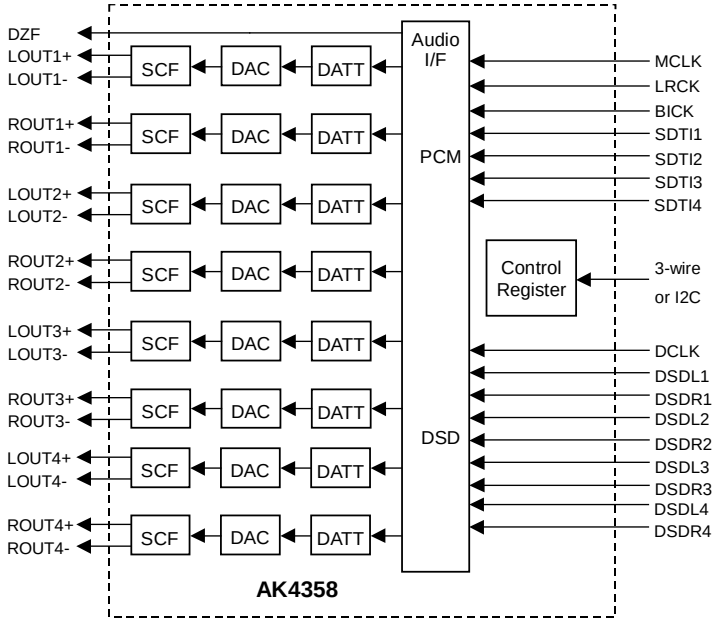
192kHz 24-Bit 8ch DAC with DSD Input

GENERAL DESCRIPTION

The AK4358 is eight channels 24bit DAC corresponding to digital audio system. Using AKM's advanced multi bit architecture for its modulator the AK4358 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4358 has full differential SCF outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The AK4358 accepts 192kHz PCM data and 1-Bit DSD data, ideal for a wide range of applications including DVD-Audio and SACD.

FEATURES

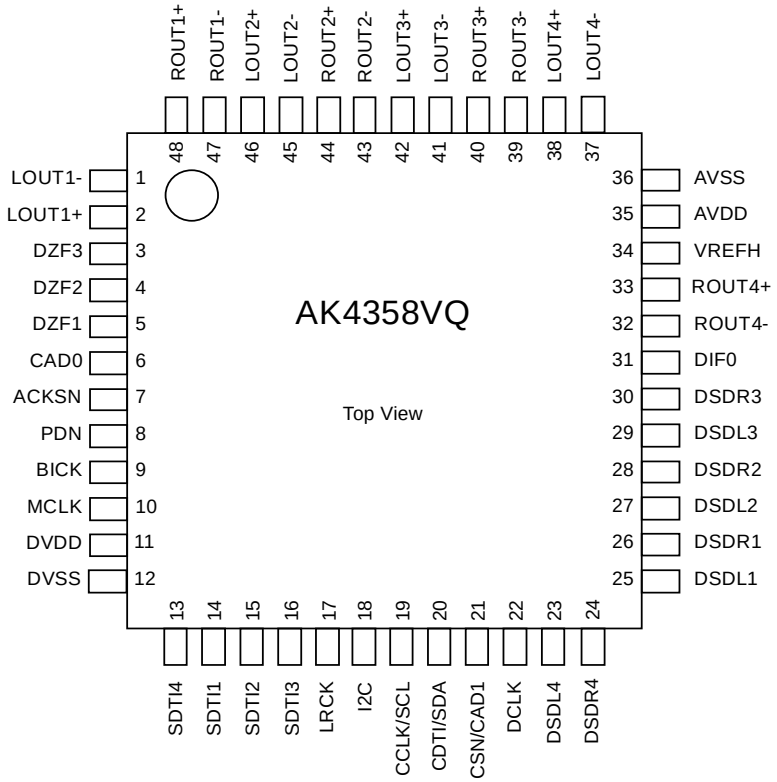
- **Sampling Rate Ranging from 8kHz to 192kHz**
- **24Bit 8 times Digital Filter with Slow roll-off option**
- **THD+N: -94dB**
- **DR, S/N: 112dB**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **DSD Data input available**
- **Digital De-emphasis for 32, 44.1 & 48kHz sampling**
- **Zero Detect function**
- **Channel Independent Digital Attenuator with soft-transition (3 Speed mode)**
- **Soft Mute**
- **3-wire Serial and I^2C Bus µP I/F for mode setting**
- **I/F format: MSB justified, LSB justified (16bit, 20bit, 24bit), I^2S, TDM or DSD**
- **Master clock: 256fs, 384fs, 512fs or 768fs (PCM Normal Speed Mode)**
  128fs, 192fs, 256fs or 384fs (PCM Double Speed Mode)
  128fs or 192fs (PCM Quad Speed Mode)
  512fs or 768fs (DSD Mode)
- **Power Supply: 4.75 to 5.25V**
- **48pin LQFP Package**



■ Ordering Guide

AK4358VQ	-40 ~ +85°C	48LQFP
AKD4358	Evaluation Board for AK4358	

■ Pin Layout



■ Compatibility with AK4357

1. Function & Performance

Functions	AK4357	AK4358
# of channels	6	8
DR	106dB	112dB
48kHz/96kHz TDM	Not available	Available
I2C	Not available	Available
DSDM control	Pin/Register	Register
Input channel of DZF pin	Fixed	Programmable

2. Pin Configuration

Pin #	AK4357	AK4358
3	DZFL1	DZF3
4	DZFR1	DZF2
5	DZF23	DZF1
7	CAD1	ACKSN
12	NC	DVSS
13	DVSS	SDTI4
18	SMUTE	I2C
19	CCLK	CCLK/SCL
20	CDTI	CDTI/SDA
21	CSN	CSN/CAD1
22	DSDM	DCLK
23	DCLK	DSDL4
24	NC	DSDR4
32	DIF1	ROUT4-
33	DIF2	ROUT4+
37	AVSS	LOUT4-
38	AVSS	LOUT4-

3. Register

Addr	Bit	AK4357	AK4358
00H	D5	DZFM	0
01H	D6	0	PW4
04H	D7	ATT7	ATTE
05H	D7	ATT7	ATTE
06H	D7	ATT7	ATTE
07H	D7	ATT7	ATTE
08H	D7	ATT7	ATTE
09H	D7	ATT7	ATTE
0AH	D7, D6	0, 0	TDM1, TDM0
0BH		Not available	LOUT4 ATT Control
0CH		Not available	ROUT4 ATT Control
0DH		Not available	DZF1 control
0EH		Not available	DZF2 control
0FH		Not available	DZF3 control

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LOUT1-	O	DAC1 Lch Negative Analog Output Pin
2	LOUT1+	O	DAC1 Lch Positive Analog Output Pin
3	DZF3	O	Zero Input Detect 3 Pin
4	DZF2	O	Zero Input Detect 2 Pin
5	DZF1	O	Zero Input Detect 1 Pin
6	CAD0	I	Chip Address 0 Pin
7	ACKSN	I	Auto Setting Mode Disable Pin (Pull-down Pin) "L": Auto Setting Mode, "H": Manual Setting Mode
8	PDN	I	Power-Down Mode Pin When at "L", the AK4358 is in the power-down mode and is held in reset. The AK4358 should always be reset upon power-up.
9	BICK	I	Audio Serial Data Clock Pin
10	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
11	DVDD	-	Digital Power Supply Pin, +4.75~+5.25V
12	DVSS	-	Digital Ground Pin
13	SDTI4	I	DAC4 Audio Serial Data Input Pin
14	SDTI1	I	DAC1 Audio Serial Data Input Pin
15	SDTI2	I	DAC2 Audio Serial Data Input Pin
16	SDTI3	I	DAC3 Audio Serial Data Input Pin
17	LRCK	I	L/R Clock Pin
18	I2C	I	Control Mode Select Pin "L": 3-wire Serial, "H": I^2C Bus
19	CCLK/SCL	I	Control Data Clock Pin I2C = "L": CCLK (3-wire Serial), I2C = "H": SCL (I^2C Bus)
20	CDTI/SDA	I/O	Control Data Input Pin I2C = "L": CDTI (3-wire Serial), I2C = "H": SDA (I^2C Bus)
21	CSN/CAD1	I	Chip Select Pin I2C = "L": CSN (3-wire Serial), I2C = "H": CAD1 (I^2C Bus)
22	DCLK	I	DSD Clock Pin
23	DSDL4	I	DAC4 DSD Lch Data Input Pin
24	DSDR4	I	DAC4 DSD Rch Data Input Pin
25	DSDL1	I	DAC1 DSD Lch Data Input Pin
26	DSDR1	I	DAC1 DSD Rch Data Input Pin
27	DSDL2	I	DAC2DSD Lch Data Input Pin
28	DSDR2	I	DAC2 DSD Rch Data Input Pin
29	DSDL3	I	DAC3 DSD Lch Data Input Pin
30	DSDR3	I	DAC3 DSD Rch Data Input Pin
31	DIF0	I	Audio Data Interface Format 0 Pin
32	ROUT4-	O	DAC4 Rch Negative Analog Output Pin
33	ROUT4+	O	DAC4 Rch Positive Analog Output Pin
34	VREFH	I	Positive Voltage Reference Input Pin
35	AVDD	-	Analog Power Supply Pin, +4.75~+5.25V
36	AVSS	-	Analog Ground Pin
37	LOUT4-	O	DAC4 Lch Negative Analog Output Pin
38	LOUT4+	O	DAC4 Lch Positive Analog Output Pin
39	ROUT3-	O	DAC3 Rch Negative Analog Output Pin
40	ROUT3+	O	DAC3 Rch Positive Analog Output Pin
41	LOUT3-	O	DAC3 Lch Negative Analog Output Pin
42	LOUT3+	O	DAC3 Lch Positive Analog Output Pin
43	ROUT2-	O	DAC2 Rch Negative Analog Output Pin
44	ROUT2+	O	DAC2 Rch Positive Analog Output Pin

45	LOUT2-	O	DAC2 Lch Negative Analog Output Pin
46	LOUT2+	O	DAC2 Lch Positive Analog Output Pin
47	ROUT1-	O	DAC1 Rch Negative Analog Output Pin
48	ROUT1+	O	DAC1 Rch Positive Analog Output Pin

Note: All input pins except pull-down pin should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	Min	Max	Units
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	|AVSS-DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Operating Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

Note 2. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies	Analog	AVDD	4.75	5.0	5.25	V
(Note 3)	Digital	DVDD	4.75	5.0	5.25	V
Voltage Reference		VREF	AVDD-0.5	-	AVDD	V

Note 3. The power up sequence between AVDD and DVDD is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=5V; VREFH=AVDD; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Input Data; Measurement frequency=20Hz ~ 20kHz; $R_L \geq 2k\Omega$; unless otherwise specified)

Parameter			Min	Typ	Max	Units
Resolution					24	Bits
Dynamic Characteristics		(Note 4)				
THD+N	fs=44.1kHz	0dBFS		-94	-86	dB
	BW=20kHz	-60dBFS		-48	-	dB
	fs=96kHz	0dBFS		-92	-84	dB
	BW=40kHz	-60dBFS		-45	-	dB
	fs=192kHz	0dBFS		-92	-	dB
	BW=40kHz	-60dBFS		-45	-	dB
Dynamic Range (-60dBFS with A-weighted)		(Note 5)	102	112		dB
S/N (A-weighted)		(Note 6)	102	112		dB
Interchannel Isolation (1kHz)			90	100		dB
Interchannel Gain Mismatch				0.2	0.5	dB
DC Accuracy						
Gain Drift				100	-	ppm/°C
Output Voltage		(Note 7)	±2.35	±2.5	±2.65	Vpp
Load Resistance		(Note 8)	2			kΩ
Power Supplies						
Power Supply Current (AVDD+DVDD)						
Normal Operation (PDN = "H", fs≤96kHz)		(Note 9)		56	70	mA
Normal Operation (PDN = "H", fs=192kHz)		(Note 10)		62	85	mA
Power-Down Mode (PDN = "L")		(Note 11)		10	100	μA

Note 4. Measured by Audio Precision System Two. Refer to the evaluation board manual.

Note 5. 100dB at 16bit data.

Note 6. S/N does not depend on input bit length.

Note 7. Full scale voltage (0dB). Output voltage scales with the voltage of VREFH pin. AOUT (typ. @0dB) = (AOUT+)-(AOUT-) = ±2.5Vpp×VREFH/5.0

Note 8. For AC-load. 4kΩ for DC-load

Note 9 AVDD=40mA(Typ), DVDD=12mA(Typ)@44.1kHz&5V, 16mA(Typ)@96kHz&5V

Note 10 AVDD=40mA(Typ), DVDD=22mA(Typ)@192kHz&5V

Note 11. All digital inputs including clock pins (MCLK, BICK and LRCK) are held DVDD or DVSS.

SHARP ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 4.75 ~ 5.25V; fs = 44.1kHz; DEM = OFF; SLOW = "0"; PCM Mode)

Parameter			Symbol	Min	Typ	Max	Units
Digital filter							
Passband ±0.05dB (Note 12)			PB	0		20.0	kHz
-6.0dB				-	22.05	-	kHz
Stopband (Note 12)			SB	24.1			kHz
Passband Ripple			PR			± 0.02	dB
Stopband Attenuation			SA	54			dB
Group Delay (Note 13)			GD	-	19.1	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	Fs=44.1kHz	FR	-	± 0.2	-	dB
	40.0kHz	Fs=96kHz	FR	-	± 0.3	-	dB
	80.0kHz	Fs=192kHz	FR	-	+0/-0.6	-	dB

Note 12. The passband and stopband frequencies scale with fs(system sampling rate). For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note 13. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 4.75~5.25V; fs = 44.1kHz; DEM = OFF; SLOW = "1"; PCM Mode)

Parameter			Symbol	Min	Typ	Max	Units
Digital Filter							
Passband ±0.04dB (Note 14)			PB	0		8.1	kHz
-3.0dB				-	18.2	-	kHz
Stopband (Note 14)			SB	39.2			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	72			dB
Group Delay (Note 13)			GD	-	19.1	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	fs=44.kHz	FR	-	+0/-5	-	dB
	40.0kHz	fs=96kHz	FR	-	+0/-4	-	dB
	80.0kHz	fs=192kHz	FR	-	+0/-5	-	dB

Note 14. The passband and stopband frequencies scale with fs. For example, PB = 0.185×fs (@±0.04dB), SB = 0.888×fs.

DC CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 4.75 ~ 5.25V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		VIH	2.2	-	-	V
Low-Level Input Voltage		VIL	-	-	0.8	V
High-Level Output Voltage	(Iout = -80μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage	(Iout = 80μA)	VOL	-		0.4	V
Input Leakage Current	(Note 15)	Iin	-	-	± 10	μA

Note 15. ACKSN pin has internal pull-down devices, nominally 100kΩ.

SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 4.75 ~ 5.25V; C_L = 20pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency	fCLK	2.048	11.2896	36.864	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency					
Normal Mode (TDM0= "L", TDM1= "L")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	60		96	kHz
Quad Speed Mode	fsq	120		192	kHz
Duty Cycle	Duty	45		55	%
TDM256 mode (TDM0= "H", TDM1= "L")					
Normal Speed Mode	fsn	32		48	kHz
High time	tLRH	3/256fs			ns
Low time	tLRL	3/256fs			ns
TDM128 mode (TDM0= "H", TDM1= "H")					
Normal Speed Mode	fsn	32		48	kHz
Double Speed Mode	fsd	60		96	kHz
High time	tLRH	3/128fs			ns
Low time	tLRL	3/128fs			ns
PCM Audio Interface Timing					
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	30			ns
Pulse Width High	tBCKH	30			ns
BICK "↑" to LRCK Edge (Note 16)	tBLR	20			ns
LRCK Edge to BICK "↑" (Note 16)	tLRB	20			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
DSD Audio Interface Timing					
DCLK Period	tDCK	1/64fs			ns
DCLK Pulse Width Low	tDCKL	160			ns
Pulse Width High	tDCKH	160			ns
DCLK Edge to DSDL/R (Note 17)	tDDD	-20		20	ns
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		100	kHz
Bus Free Time Between Transmissions	tBUF	4.7		-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	4.0		-	μs
Clock Low Time	tLOW	4.7		-	μs
Clock High Time	tHIGH	4.0		-	μs
Setup Time for Repeated Start Condition	tSU:STA	4.7		-	μs
SDA Hold Time from SCL Falling (Note 18)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.25		-	μs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	μs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	μs
Setup Time for Stop Condition	tSU:STO	4.0		-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns

Parameter		Symbol	Min	Typ	Max	Units
Reset Timing						
PDN Pulse Width	(Note 19)	tPD	150			ns

Note 16. BICK rising edge must not occur at the same time as LRCK edge.

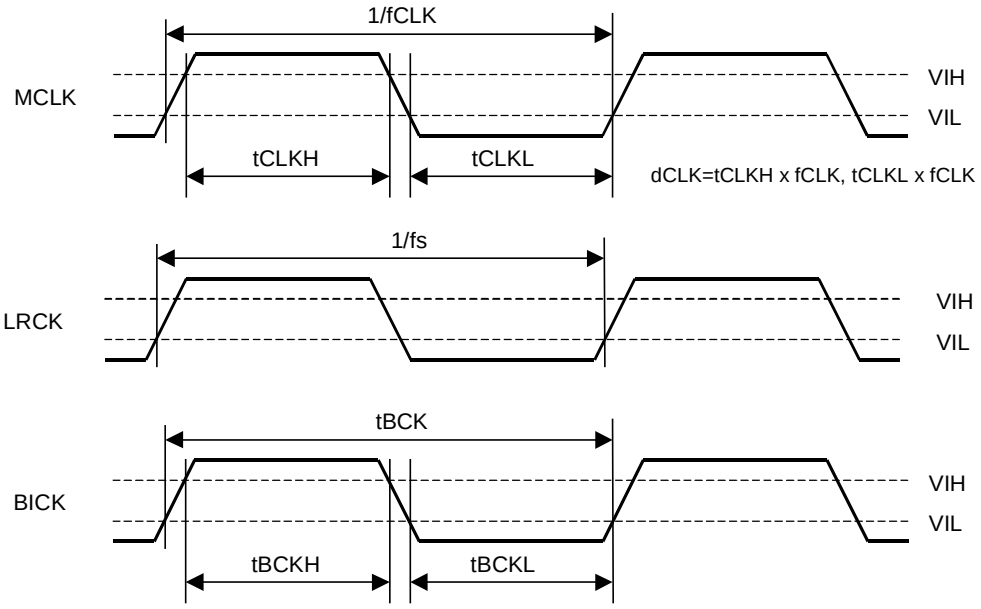
Note 17. DSD data transmitting device must meet this time.

Note 18. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

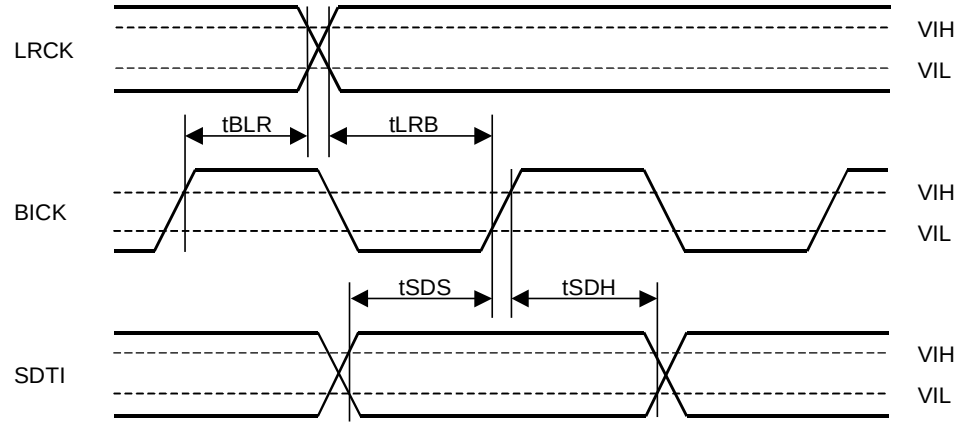
Note 19. The AK4358 can be reset by bringing PDN= "L".

Note 20. I^2C is a registered trademark of Philips Semiconductors.

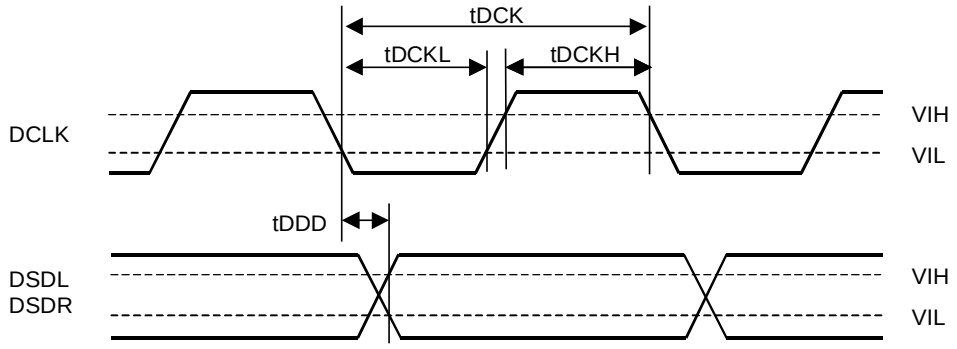
■ Timing Diagram



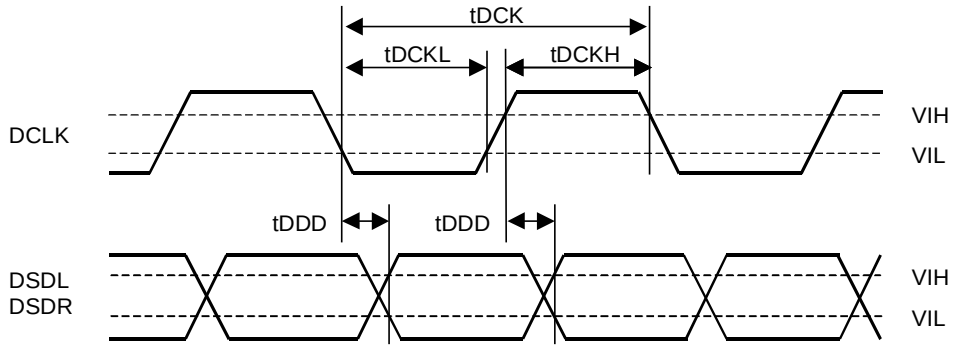
Clock Timing



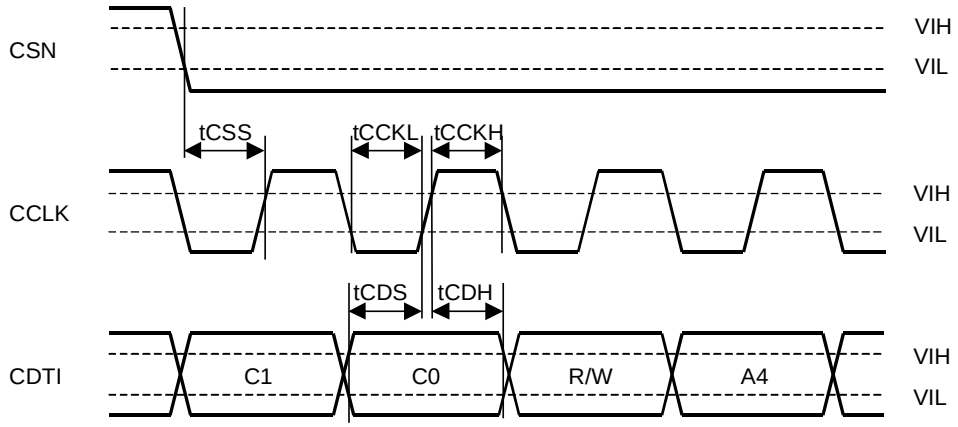
Audio Serial Interface Timing (PCM Mode)



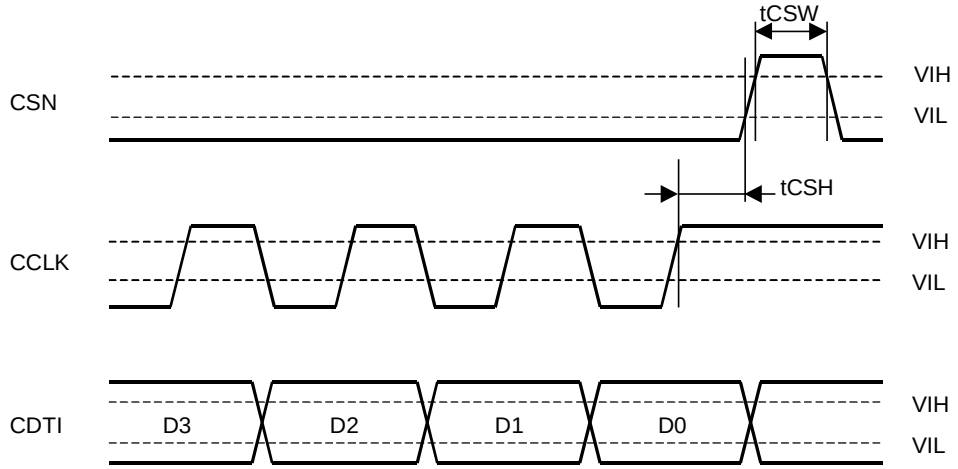
Audio Serial Interface Timing (DSD Normal Mode, DCKB = "0")



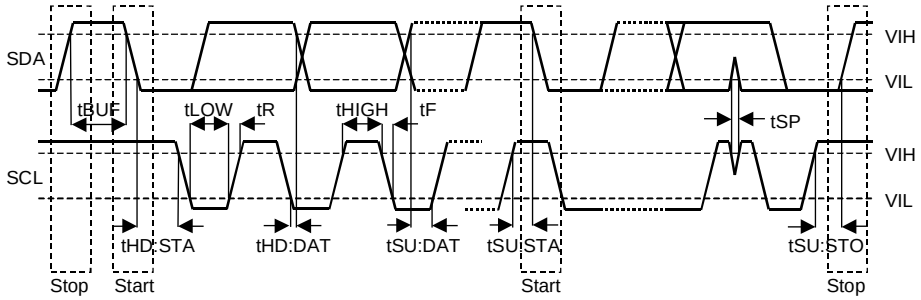
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB = "0")



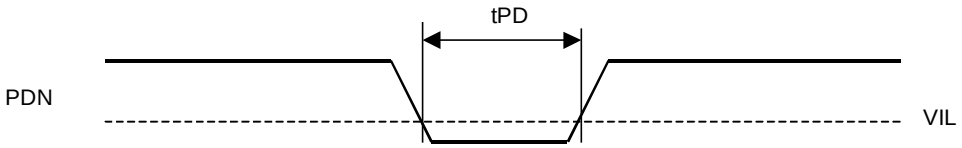
WRITE Command Input Timing



WRITE Data Input Timing



I^2C Bus mode Timing



Power-down Timing

OPERATION OVERVIEW

■ D/A Conversion Mode

The AK4358 can perform D/A conversion for both PCM data and DSD data. When DSD mode, DSD data can be input from DCLK, DSDL1-4 and DSDR1-4 pins. When PCM mode, PCM data can be input from BICK, SDTI1-4 and LRCK pins. PCM/DSD mode changes by D/P bit. When PCM/DSD mode changes by D/P bit, the AK4358 should be reset by RSTN bit, PW bit (PW1=PW2=PW3=PW4= "0") or PDN pin. It takes about 2/fs to 3/fs to change the mode.

D/P bit	DAC Output
0	PCM
1	DSD

Table 1. DSD/PCM Mode Control

■ System Clock

1) PCM Mode

The external clocks, which are required to operate the AK4358, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS = "0": Register 00H), the sampling speed is set by DFS0/1(Table 2). The frequency of MCLK at each sampling speed is set automatically. (Table 3~Table 5). In Auto Setting Mode (ACKS = "1": Default), as MCLK frequency is detected automatically (Table 6), and the internal master clock becomes the appropriate frequency (Table 7), it is not necessary to set DFS0/1. When ACKSN = "H", regardless of ACKS bit setting the AK4358 operates by Manual Setting Mode. When ACKSN = "L", ACKS bit setting is valid.

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4358 is in the normal operation mode (PDN= "H"). If these clocks are not provided, the AK4358 may draw excess current and may fall into unpredictable operation. This is because the device utilizes dynamic refreshed logic internally. The AK4358 should be reset by PDN = "L" after threse clocks are provided. If the external clocks are not present, the AK4358 should be in the power-down mode (PDN= "L"). After exiting reset(PDN = "↑") at power-up etc., the AK4358 is in the power-down mode until MCLK is input. DSD interface signals (DCLK, DSDL1-4, DSDR1-4) are fixed to "H" or "L".

DFS1	DFS0	Sampling Rate (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	Default
0	1	Double Speed Mode	60kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 2. Sampling Speed (Manual Setting Mode)

LRCK	MCLK				BICK
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	3.0720MHz

Table 3. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 4. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK		BICK
fs	128fs	192fs	64fs
176.4kHz	22.5792MHz	33.8688MHz	11.2896MHz
192.0kHz	24.5760MHz	36.8640MHz	12.2880MHz

Table 5. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK		Sampling Speed
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 6. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	-	-	16.3840	24.5760	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	

Table 7. System Clock Example (Auto Setting Mode)

ACKSN pin	ACKS bit	Clock Mode	
0	0	Manual Setting Mode	
0	1	Auto Setting Mode	(Default)
1	0	Manual Setting Mode	
1	1	Manual Setting Mode	

Table 8. Relationship between ACKSN pin and ACKS bit

2) DSD Mode

The external clocks, which are required to operate the AK4358, are MCLK and DCLK. The master clock (MCLK) should be synchronized with DSD clock (DCLK) but the phase is not critical. The frequency of MCLK is set by DCKS bit.

All external clocks (MCLK, DCLK) should always be present whenever the AK4358 is in the normal operation mode (PDN= ”H”). If these clocks are not provided, the AK4358 may draw excess current because the device utilizes dynamic refreshed logic internally. The AK4358 should be reset by PDN= ”L” after threse clocks are provided. If the external clocks are not present, the AK4358 should be in the power-down mode (PDN= ”L”). After exiting reset(PDN = “↑”) at power-up etc., the AK4358 is in the power-down mode until MCLK is input. PCM interface signals (BICK, LRCK, SDTI1-4) are fixed to “H” or “L”.

DCKS	0	1
MCLK	512fs	768fs
DCLK	64fs	64fs

Table 9. System Clock (fs=44.1kHz)

■ Audio Serial Interface Format

1) PCM Mode

When PCM mode, data is shifted in via the SDTI1-4 pins using BICK and LRCK inputs. The DIF0-2 as shown in Table 10 can select five serial data modes. Initial value of DIF0-2 bits is "010" and DIF0 bit is ORed with DIF0 pin. In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 16/20 MSB justified formats by zeroing the unused LSBs.

When TDM0 = "1", the audio interface becomes TDM mode. In TDM256 mode (TDM1 = "0", Table 11), the serial data of all DAC (eight channels) is input to the SDTI1 pin. The input data to SDTI2-4 pins is ignored. BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be 3/256fs at least. The serial data is MSB-first, 2's compliment format. The input data to SDTI1 pin is latched on the rising edge of BICK. In TDM128 mode (TDM1 = "1", Table 12), the serial data of DAC (four channels; L1, R1, L2, R2) is input to the SDTI1 pin. Other four data (L3, R3, L4, R4) is input to the SDTI2. The input data to SDTI3-4 pins is ignored. BICK should be fixed to 128fs.

Mode	TDM1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK	Figure	
0	0	0	0	0	0	16bit LSB Justified	H/L	≥32fs	Figure 1	
1	0	0	0	0	1	20bit LSB Justified	H/L	≥40fs	Figure 2	
2	0	0	0	1	0	24bit MSB Justified	H/L	≥48fs	Figure 3	Default
3	0	0	0	1	1	24bit I^2S Compatible	L/H	≥48fs	Figure 4	
4	0	0	1	0	0	24bit LSB Justified	H/L	≥48fs	Figure 2	

Table 10. Audio Data Formats (Normal mode)

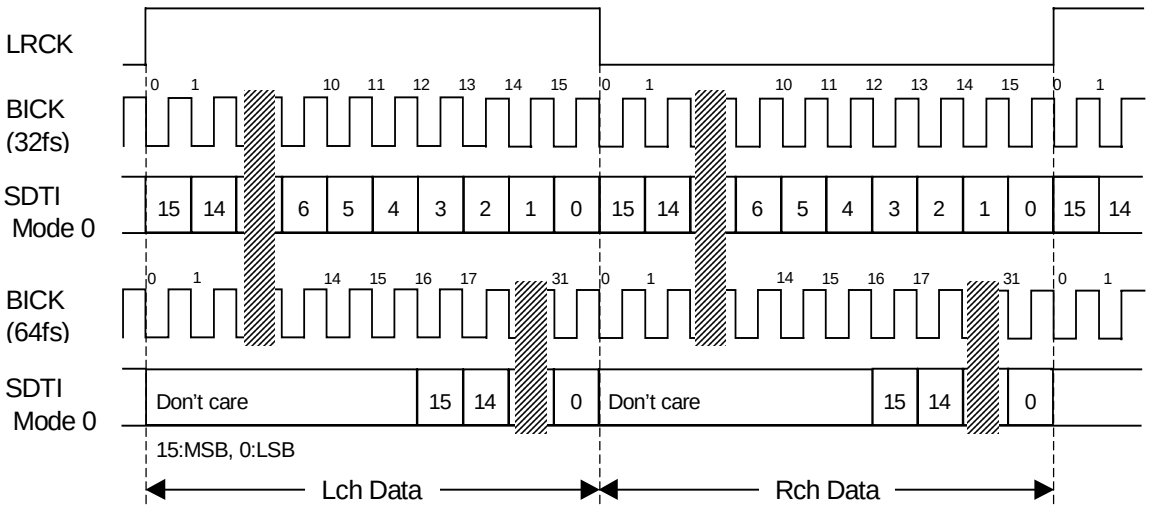


Figure 1. Mode 0 Timing

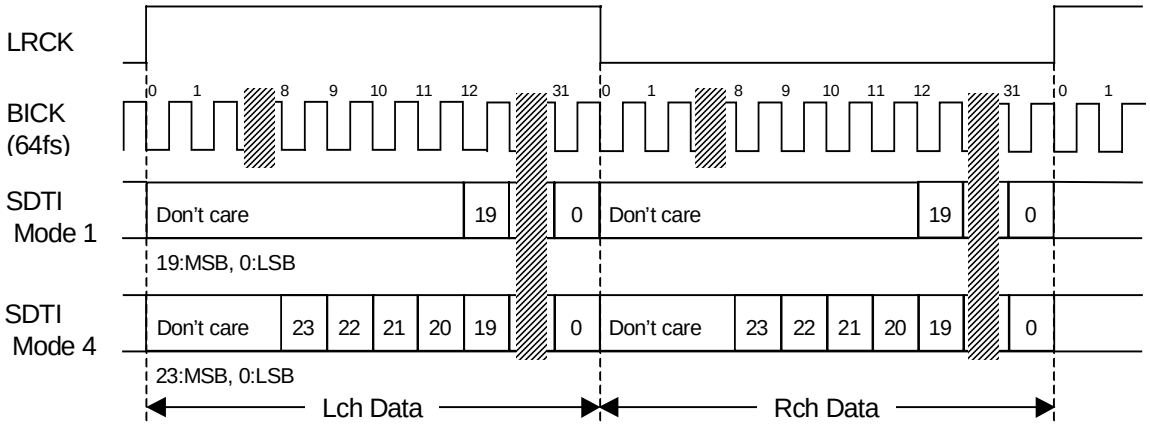


Figure 2. Mode 1,4 Timing

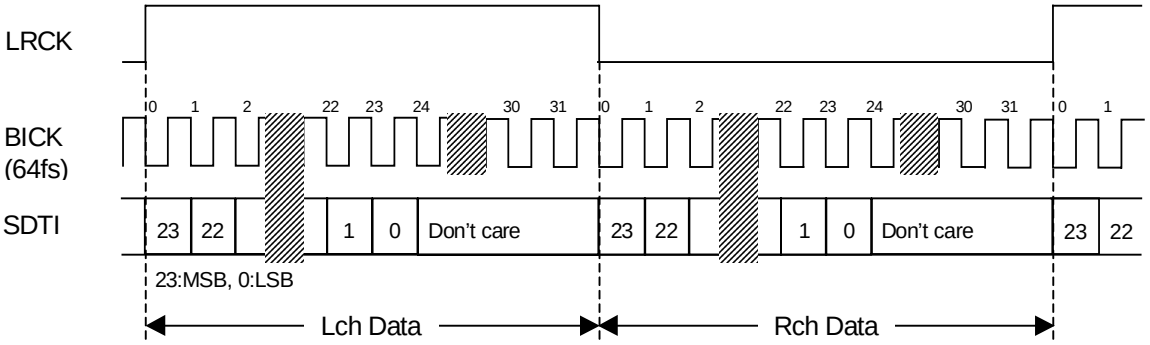


Figure 3. Mode 2 Timing

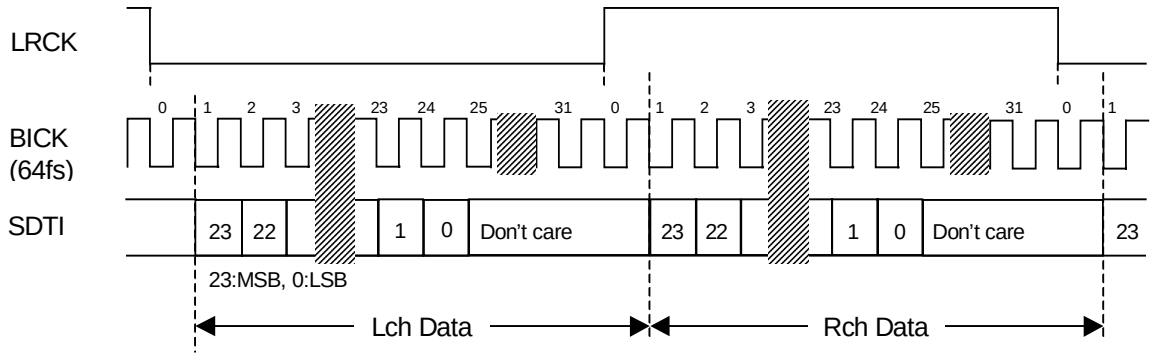


Figure 4. Mode 3 Timing

Mode	TDM1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK	Figure
	0	1	0	0	0	N/A			
	0	1	0	0	1	N/A			
5	0	1	0	1	0	24bit MSB Justified	↑	256fs	Figure 5
6	0	1	0	1	1	24bit I^2S Compatible	↓	256fs	Figure 6
7	0	1	1	0	0	24bit LSB Justified	↑	256fs	Figure 7

Table 11. Audio Data Formats (TDM256 mode)

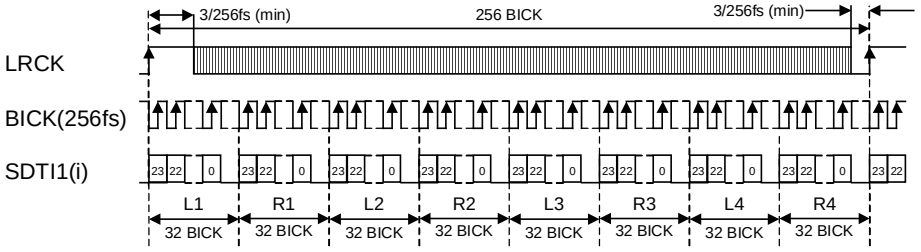


Figure 5. Mode 5 Timing

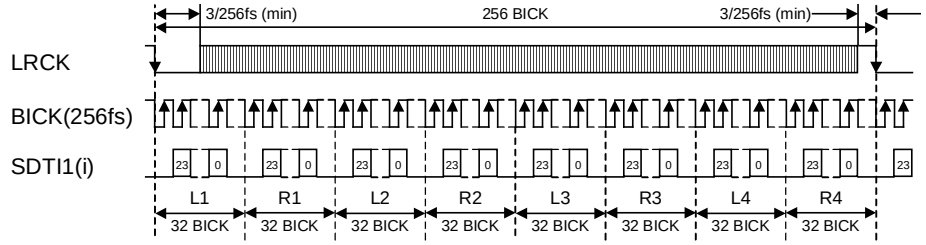


Figure 6. Mode 6 Timing

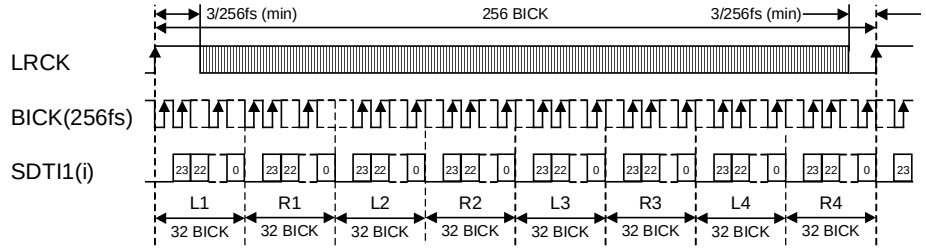


Figure 7. Mode 7 Timing

Mode	TDM1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK	Figure
	1	1	0	0	0	N/A			
	1	1	0	0	1	N/A			
8	1	1	0	1	0	24bit MSB Justified	↑	128fs	Figure 8
9	1	1	0	1	1	24bit I^2S Compatible	↓	128fs	Figure 9
10	1	1	1	0	0	24bit LSB Justified	↑	128fs	Figure 10

Table 12. Audio Data Formats (TDM128 mode)

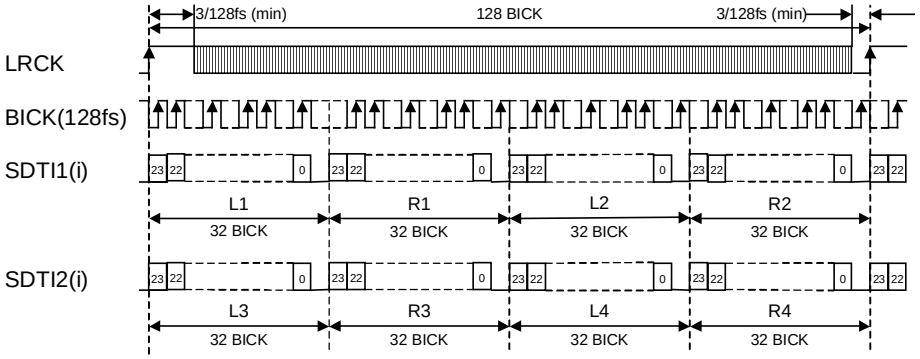


Figure 8. Mode 8 Timing

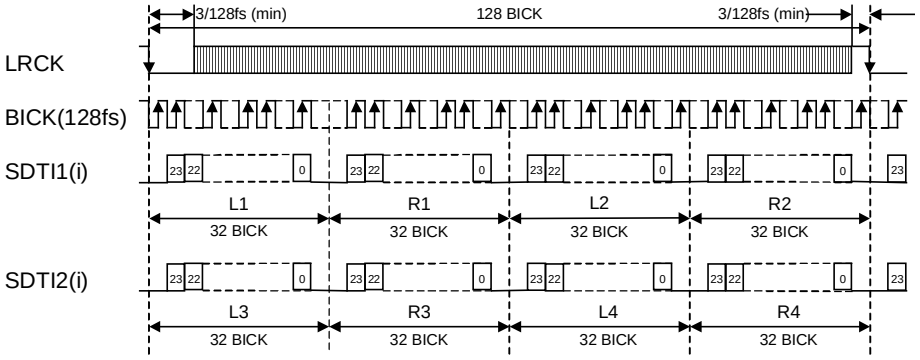


Figure 9. Mode 9 Timing

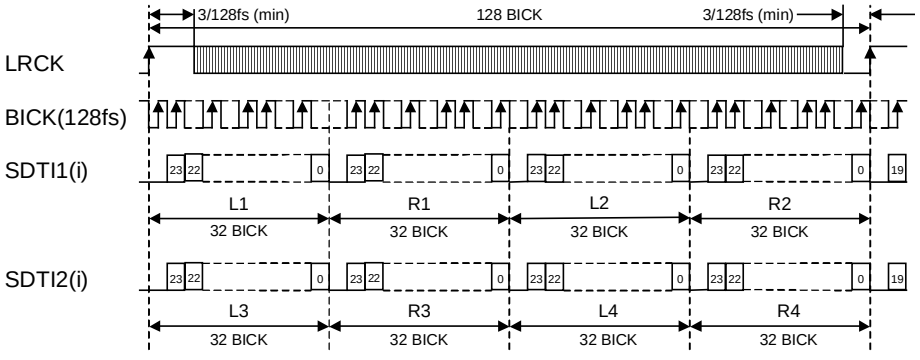


Figure 10. Mode 10 Timing

2) DSD Mode

In case of DSD mode, DIF0-2 is ignored. The frequency of DCLK is fixed to 64fs. DCKB bit can invert the polarity of DCLK.

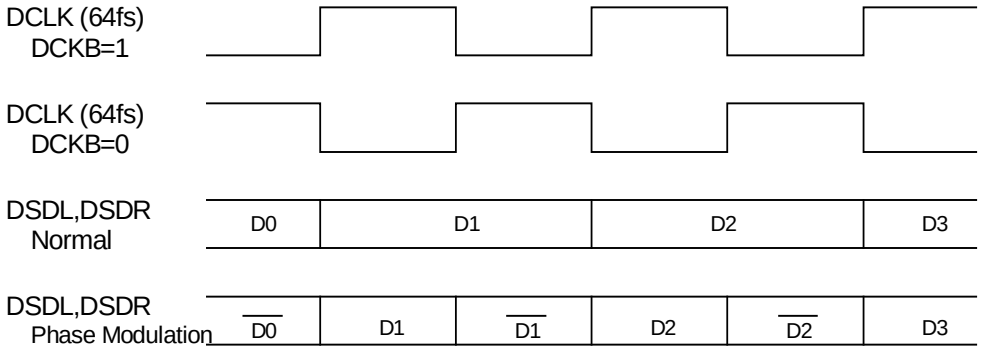


Figure 11. DSD Mode Timing

■ D/A conversion mode switching timing

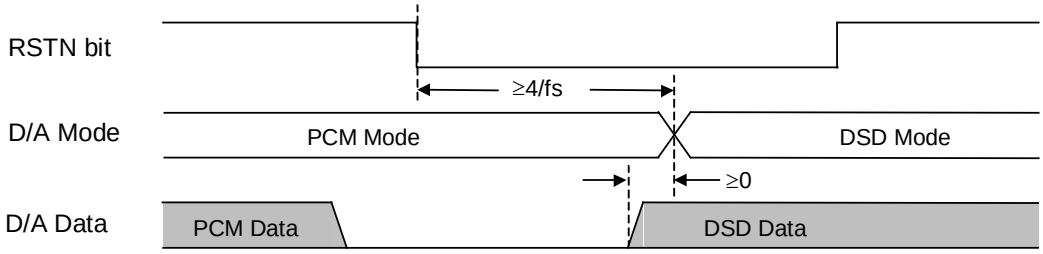


Figure 12. D/A Mode Switching Timing (PCM to DSD)

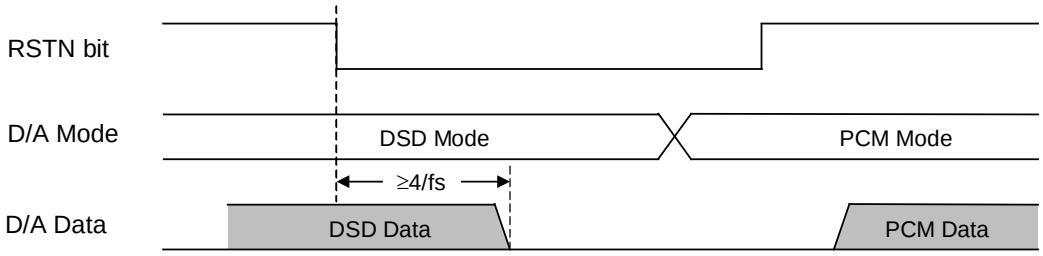


Figure 13. D/A Mode Switching Mode Timing (DSD to PCM)

Caution: In DSD mode, the signal level is ranging from 25% to 75%. Peak levels of DSD signal above this duty are not recommended by SACD format book (Scarlet Book).

■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc = 50/15μs) and is enabled or disabled with DEM0 and DEM1. In case of double speed and quad speed mode, the digital de-emphasis filter is always off. When DSD mode, DEM0-1 is invalid.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 13. De-emphasis Filter Control (Normal Speed Mode)

■ Output Volume

The AK4358 includes channel independent digital output volumes (ATT) with 128 levels at 0.5dB steps including SMUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to –63dB and mute. Transition time is set by AST1-0 bits(Table 15) When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. When ATTE bit is set to "0", the DAC input data goes to "0" immediately. It takes a time of group delay to mute the analog output. ATTE bit should be "1" to enable the volume setting.

ATTE	ATT6-0	Attenuation Level	
1	7FH	0dB	Default
	7EH	-0.5dB	
	7DH	-1.0dB	
	:	:	
	02H	-62.5dB	
	01H	-63.0dB	
	00H	SMUTE (-∞)	
0	Don't care	OFF ("0")	

Table 14. Attenuation Level of Output Volume

Mode	ATS1	ATS0	ATT speed	
0	0	0	1792/fs	Default
1	0	1	896/fs	
2	1	0	256/fs	
3	1	1	N/A	

Table 15. Transition time of output volume

In case of Mode 0, it takes 1792/fs to transit from 7FH(0dB) to 00H(SMUTE). In case Mode1, it takes 896/fs to transit from 7FH(0dB) to 00H(SMUTE). In case Mode2 and 3,it takes 256/fs to transit from 7FH(0dB) to 00H (SMUTE). If PDN pin goes to "L", ATT6-0 registers are initialized to 7FH.ATT6-0 registers go to 7FH when RSTN bit is set to "0". When RSTN bit returns to "1", ATT6-0 registers go to the set value. Digital output volume function is independent of soft mute function.

The setting value of the register is held when switching between PCM mode and DSD mode.

■ Zero Detection

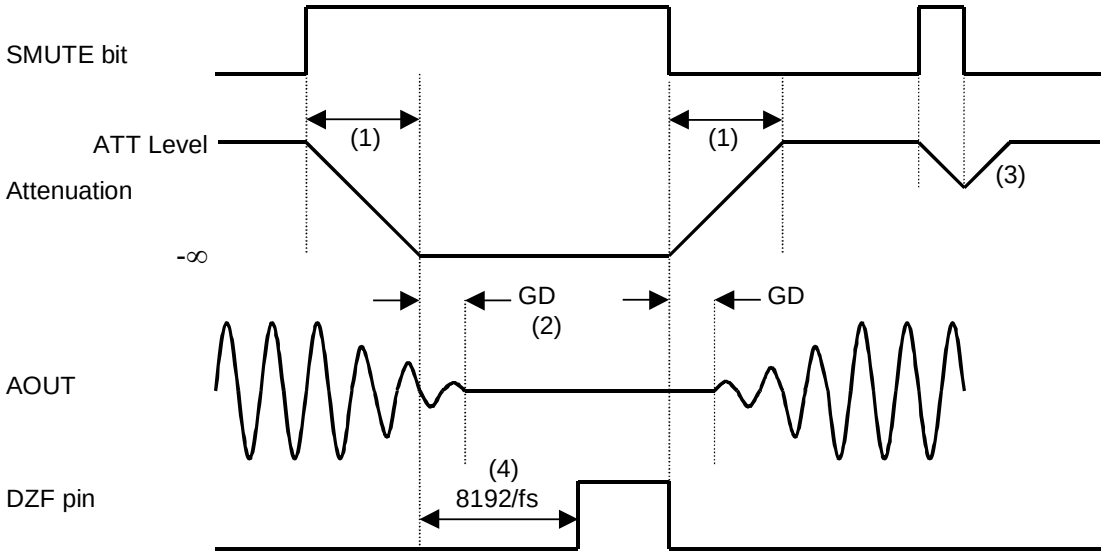
When the input data at all channels are continuously zeros for 8192 LRCK cycles, the AK4358 has Zero Detection like Table 16. DZF pin immediately goes to "L" if input data of each channel is not zero after going DZF "H". If RSTN bit is "0", DZF pin goes to "H". DZF pin goes to "L" at 4~5LRCK if input data of each channel is not zero after RSTN bit returns to "1". Zero detect function can be disabled by DZFE bit. In this case, all DZF pins are always "L". When one of PW1-4 bit is set to "0", the input data of DAC that the PW bit is set to "0" should be zero in order to enable zero detection of the other channels. When all PW1-4 bits are set to "0", DZF pin fixes "L". DZFB bit can invert the polarity of DZF pin.

DZF Pin	Operations
DZF1	ANDed output of zero detection flag of each channel set to "1" in 0DH register
DZF2	ANDed output of zero detection flag of each channel set to "1" in 0EH register
DZF3	ANDed output of zero detection flag of each channel set to "1" in 0FH register

Table 16. DZF pins Operation

■ Soft Mute Operation

Soft mute operation is performed at digital domain. When the SMUTE bit goes to "1", the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 15) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 15). For example, in Normal Speed Mode, this time is 1792LRCK cycles (1792/fs) at ATT_DATA=128.

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data at each channel is continuously zeros for 8192 LRCK cycles, DZF pin of each channel goes to "H". DZF pin immediately goes to "L" if input data are not zero after going DZF "H".

Figure 14. Soft Mute and Zero Detection

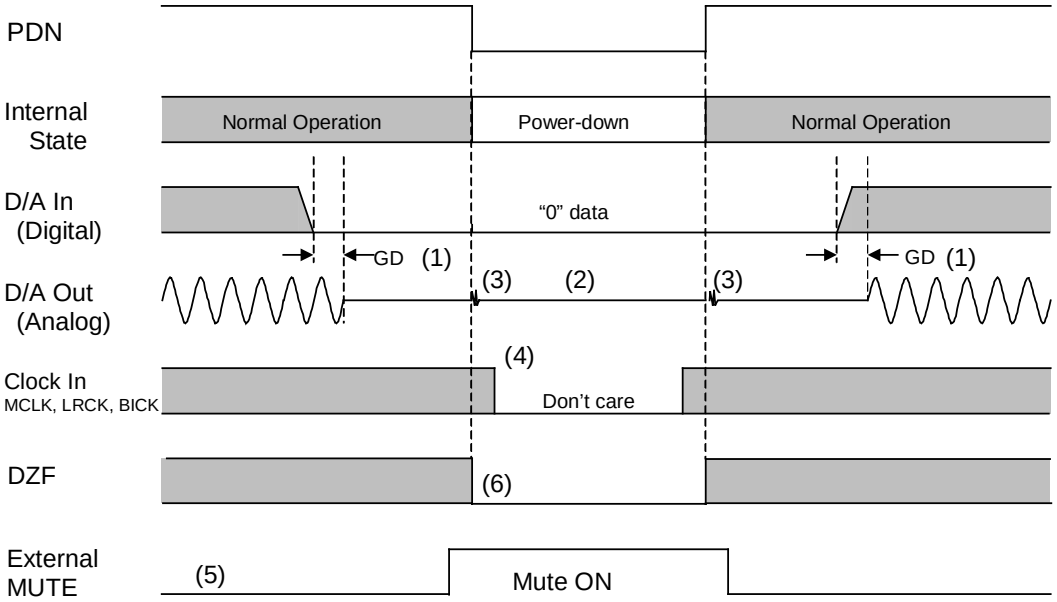
■ System Reset

The AK4358 should be reset once by bringing PDN= ”L” upon power-up. The analog section exits power-down mode by MCLK input and then the digital section exits power-down mode after the internal counter counts MCLK during 4/fs.

■ Power-down

The AK4358 is placed in the power-down mode by bringing PDN pin “L” and the anlog outputs are floating (Hi-Z). Figure 6 shows an example of the system timing at the power-down and power-up.

Each DAC can be powered down by each power-down bit (PW1-3) “0”. In this case, the internal register values are not initialized and the analog output is Hi-Z. Because some click noise occurs, the analog output should be muted externally if the click noise influences system application.



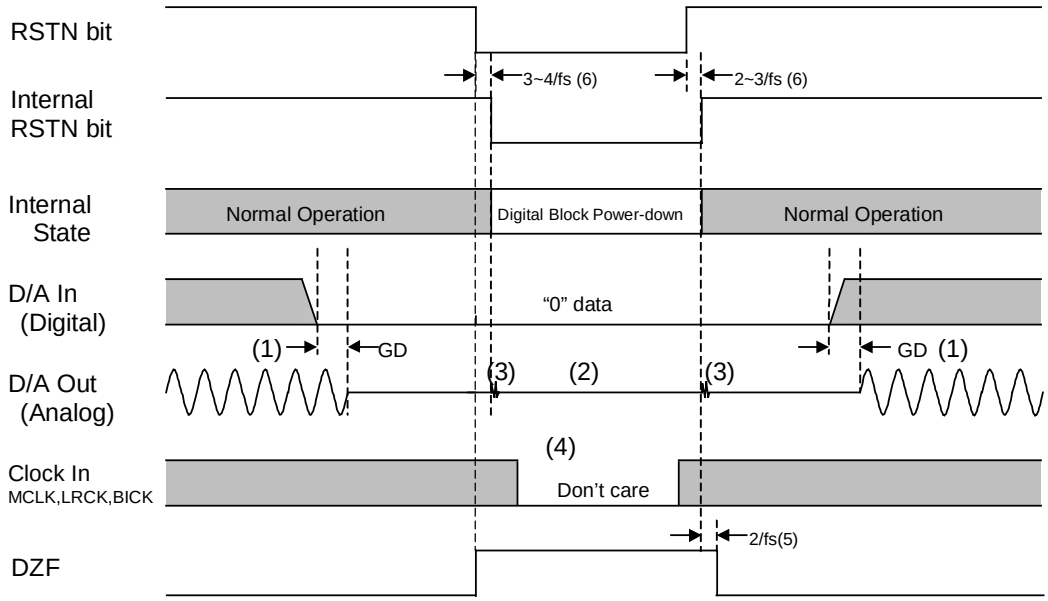
Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi -Z) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = “L”).
(5) Please mute the analog output externally if the click noise (3) influence system application. The timing example is shown in this figure.
(6) DZF pins are “L” in the power-down mode (PDN = “L”).

Figure 15. Power-down/up Sequence Example

■ Reset Function

When RSTN=0, DAC is powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage and DZFL/DZFR pins go to "H". Figure 16 shows the example of reset by RSTN bit.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs go to VCOM voltage.
(3) Click noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode (RSTN = "L").
(5) DZF pins go to "H" when the RSTN bit becomes "0", and go to "L" at 2/fs after RSTN bit becomes "1".
(6) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2~3/fs from RSTN bit "1" to the internal RSTN "1".

Figure 16. Reset Sequence Example

■ Register Control Interface

The AK4358 controls its functions via registers. 2 types of control mode write internal registers. In the I^2C-bus mode, the chip address is determined by the state of the CAD0 and CAD1 inputs. In 3-wire mode, the CAD1 input is fixed to "1" and Chip Address C0 is determined by the state of the CAD0 pin. PDN = "L" initializes the registers to their default values. Writing "0" to the RSTN bit resets the internal timing circuit, but the register data is not initialized.

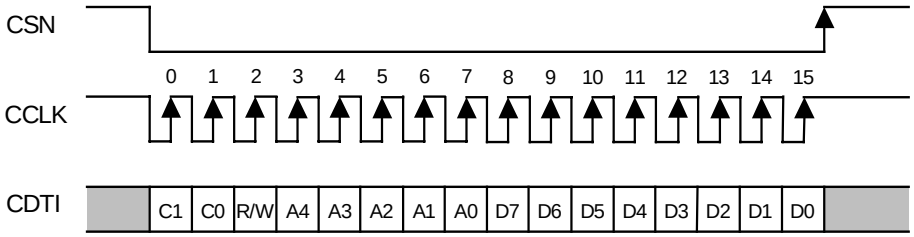
* The AK4358 does not support the read command.
* When the AK4358 is in the power down mode (PDN = "L") or the MCLK is not provided, Writing to control register is invalid.

Function	Pin set-up	Register set-up
Manual Setting Mode	O	O
De-emphasis	X	O
DZFE	X	O
SMUTE	X	O
Audio data format	DIF0	O
DSD mode	X	O
Attenuator	X	O
Slow roll-off response	X	O

Table 17. Function Table (O: Supported, X: Not supported)

(1) 3-wire Serial Control Mode (I2C = "L")

3-wire µP interface pins, CSN, CCLK and CDTI, write internal registers. The data on this interface consists of Chip Address (2bits, C1/0; C1 is fixed to "1" and C0=CAD0), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). The AK4358 latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by the rising edge of CSN. The clock speed of CCLK is 5MHz (max).



C1-C0: Chip Address (C1= "1", C0=CAD0)
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 17. Control I/F Timing

(2) I²C-bus Control Mode (I2C= "H")

The AK4358 supports the standard-mode I²C-bus (max:100kHz). Then the AK4358 does not support a fast-mode I²C-bus system (max: 400kHz).

Figure 18 shows the data transfer sequence at the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 22). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) (Figure 19). The most significant five bits of the slave address are fixed as "00100". The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The hard-wired input pins (CAD1 pin and CAD0 pin) set them. If the slave address match that of the AK4358 and R/W bit is "0", the AK4358 generates the acknowledge and the write operation is executed. If R/W bit is "1", the AK4358 generates the not acknowledge since the AK4358 can be only a slave-receiver. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 23).

The second byte consists of the address for control registers of the AK4358. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 20). Those data after the second byte contain control data. The format is MSB first, 8bits (Figure 21). The AK4358 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 22).

The AK4358 is capable of more than one byte write operation by one sequence. After receipt of the third byte, the AK4358 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the addresses exceed 1FH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 24) except for the START and the STOP condition.

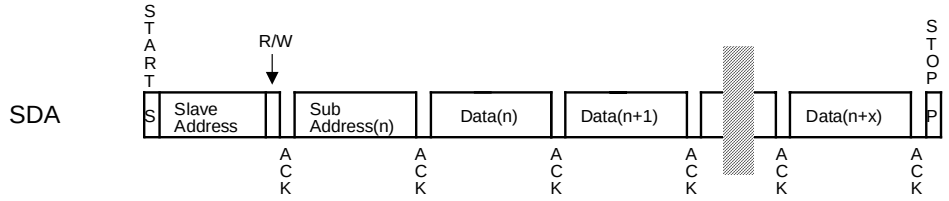


Figure 18. Data transfer sequence at the I²C-bus mode

0	0	1	0	0	CAD1	CAD0	R/W

(Those CAD1/0 should match with CAD1/0 pins)

Figure 19. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 20. The second byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 21. Byte structure after the second byte

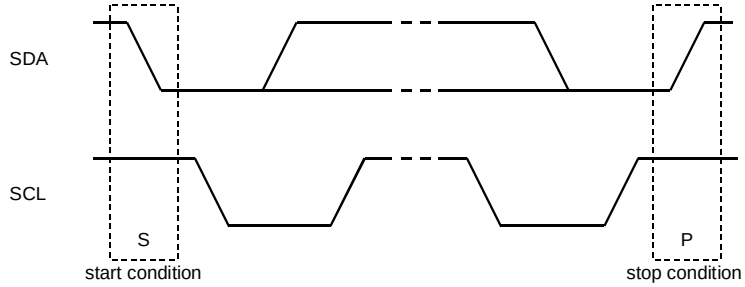


Figure 22. START and STOP conditions

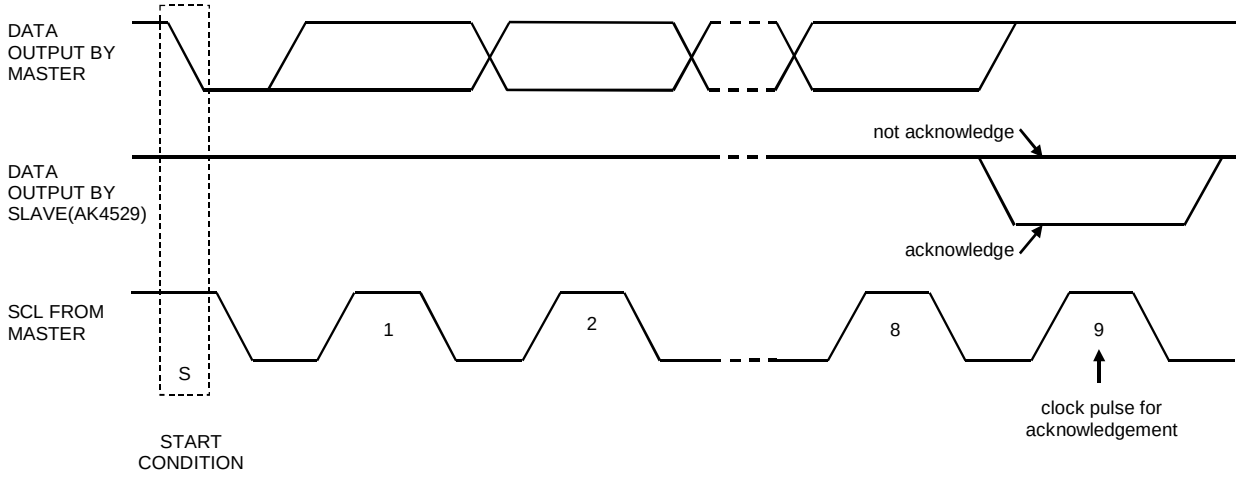


Figure 23. Acknowledge on the I^2C-bus

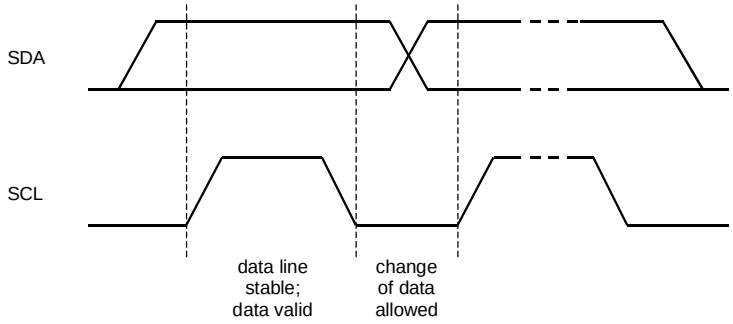


Figure 24. Bit transfer on the I^2C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	SLOW	0	DZFE	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	0	0	0	0	SMUTE	RSTN
02H	Speed & Power Down Control	0	PW4	DFS1	DFS0	PW3	PW2	PW1	RSTN
03H	De-emphasis Control	0	0	0	0	0	0	DEM1	DEM0
04H	LOUT1 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	ROUT1 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	LOUT2 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	ROUT2 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
08H	LOUT3 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
09H	ROUT3 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0AH	Control 3	TDM1	TDM0	DCKS	D/P	DCKB	DZFB	ATS1	ATS0
0BH	LOUT4 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0CH	ROUT4 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0DH	DZF1 Control	L1	R1	L2	R2	L3	R3	L4	R4
0EH	DZF2 Control	L1	R1	L2	R2	L3	R3	L4	R4
0FH	DZF3 Control	L1	R1	L2	R2	L3	R3	L4	R4

Note: For addresses from 10H to 1FH, data must not be written.
When PDN goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the only internal timing is reset, and the registers are not initialized to their default values. All data can be written to the registers even if PW1-4 or RSTN bit is “0”.
ACKS bit is ANDed with the ACKSN pin.
DIF0 bit is ORed with the DIF pin.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	SLOW	0	DZFE	DIF2	DIF1	DIF0	RSTN
Default		1	0	0	1	0	1	0	1

RSTN: Internal timing reset
0: Reset. All DZF pins go to “H” and any registers are not initialized.
1: Normal operation
When MCLK frequency or DFS changes, the AK4358 should be reset by PDN pin or RSTN bit.

DIF2-0: Audio data interface modes (See Table 10, Table 11, Table 12, PCM Only)
Initial: “010”
Register bit of DIF0 is ORed with the DIF0 pin.

DZFE: Data Zero Detect Enable
0: Disable
1: Enable
Zero detect function can be disabled by DZFE bit “0”. In this case, the DZF pins are “L” at DZFB bit “0” and are “H” at DZFB bit “1”.

SLOW: Slow Roll-off Filter Enable (PCM Only)
0: Sharp Roll-off Filter
1: Slow Roll-off Filter

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit “1”. In this case, the setting of DFS1-0 is ignored. When this bit is “0”, DFS1-0 set the sampling speed mode.
Register bit of ACKS is ANDed with the inverted of the ACKSN pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	0	0	0	0	SMUTE	RSTN
Default		0	0	0	0	0	0	0	1

RSTN: Internal timing reset
0: Reset. All DZF pins of go to “H” and any registers are not initialized.
1: Normal operation
When MCLK frequency or DFS changes, the AK4358 should be reset by PDN pin or RSTN bit.

SMUTE: Soft Mute Enable
0: Normal operation
1: All DAC outputs soft-muted

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Speed & Power Down Control	0	PW4	DFS1	DFS0	PW3	PW2	PW1	RSTN
Default		0	1	0	0	1	1	1	1

RSTN: Internal timing reset
0: Reset. All DZF pins go to "H" and any registers are not initialized.
1: Normal operation
When MCLK frequency or DFS changes, the AK4358 should be reset by PDN pin or RSTN bit.

PW4-1: Power-down control (0: Power-down, 1: Power-up)
PW1: Power down control of DAC1
PW2: Power down control of DAC2
PW3: Power down control of DAC3
PW4: Power down control of DAC4
All sections are powered-down by PW1=PW2=PW3=PW4=0.

DFS1-0: Sampling speed control (See Table 2, PCM Only)
00: Normal speed
01: Double speed
10: Quad speed
When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	De-emphasis Control	0	0	0	0	0	0	DEM1	DEM0
Default		0	0	0	0	0	0	0	1

DEM1-0: De-emphasis response control for DAC1/2/3/4 data on SDTI1/2/3/4 (See Table 13, PCM only)
Initial: "01", OFF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	LOUT1 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	ROUT1 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	LOUT2 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	ROUT2 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
08H	LOUT3 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
09H	ROUT3 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0BH	LOUT4 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0CH	ROUT4 ATT Control	ATTE	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
Default		1	1	1	1	1	1	1	1

ATT6-0: Attenuation Level
128 levels, 0.5dB step (See Table 14)

ATTE: Attenuation Output Enable
0: Disable
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control 3	TDM1	TDM0	DCKS	D/P	DCKB	DZFB	ATS1	ATS0
Default		0	0	0	0	0	0	0	0

ATS1-0: DATT Speed Setting (See Table 15)
Initial: "00", mode 0

DZFB: Inverting Enable of DZF
0: DZF goes "H" at Zero Detection
1: DZF goes "L" at Zero Detection

DCKB: Polarity of DCLK (DSD Only)
0: DSD data is output from DCLK falling edge
1: DSD data is output from DCLK rising edge

D/P: DSD/PCM Mode Select
0: PCM Mode. SCLK, SDTI1-4, LRCK
1: DSD Mode. DCLK, DSDL1-4, DSDR1-4
When D/P changes form "1" to "0", the AK4358 should be reset by PDN pin, PW bit or RSTN bit.
When D/P changes form "0" to "1", the AK4358 should be reset by PW bit or RSTN bit.

DCKS: Master Clock Frequency Select at DSD mode (DSD only)
0: 512fs
1: 768fs

TDM0-1: TDM Mode Select (PCM only)

Mode	TDM1	TDM0	BICK	SDTI	Sampling Speed
Normal	0	0	32fs~	1-4	Normal, Double, Quad Speed
TDM256	0	1	256fs fixed	1	Normal Speed
TDM128	1	1	128fs fixed	1-2	Normal, Double Speed

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	DZF1 Control	L1	R1	L2	R2	L3	R3	L4	R4
Default		1	1	1	1	1	1	1	1

L1-4, R1-4: Zero Detect Flag Enable Bit for DZF1 pin
0: Disable
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	DZF2 Control	L1	R1	L2	R2	L3	R3	L4	R4
0FH	DZF3 Control	L1	R1	L2	R2	L3	R3	L4	R4
Default		0	0	0	0	0	0	0	0

L1-4, R1-4: Zero Detect Flag Enable Bit for DZF2,3 pins
0: Disable
1: Enable

SYSTEM DESIGN

Figure 25 shows the system connection diagram. An evaluation board (AKD4358) is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

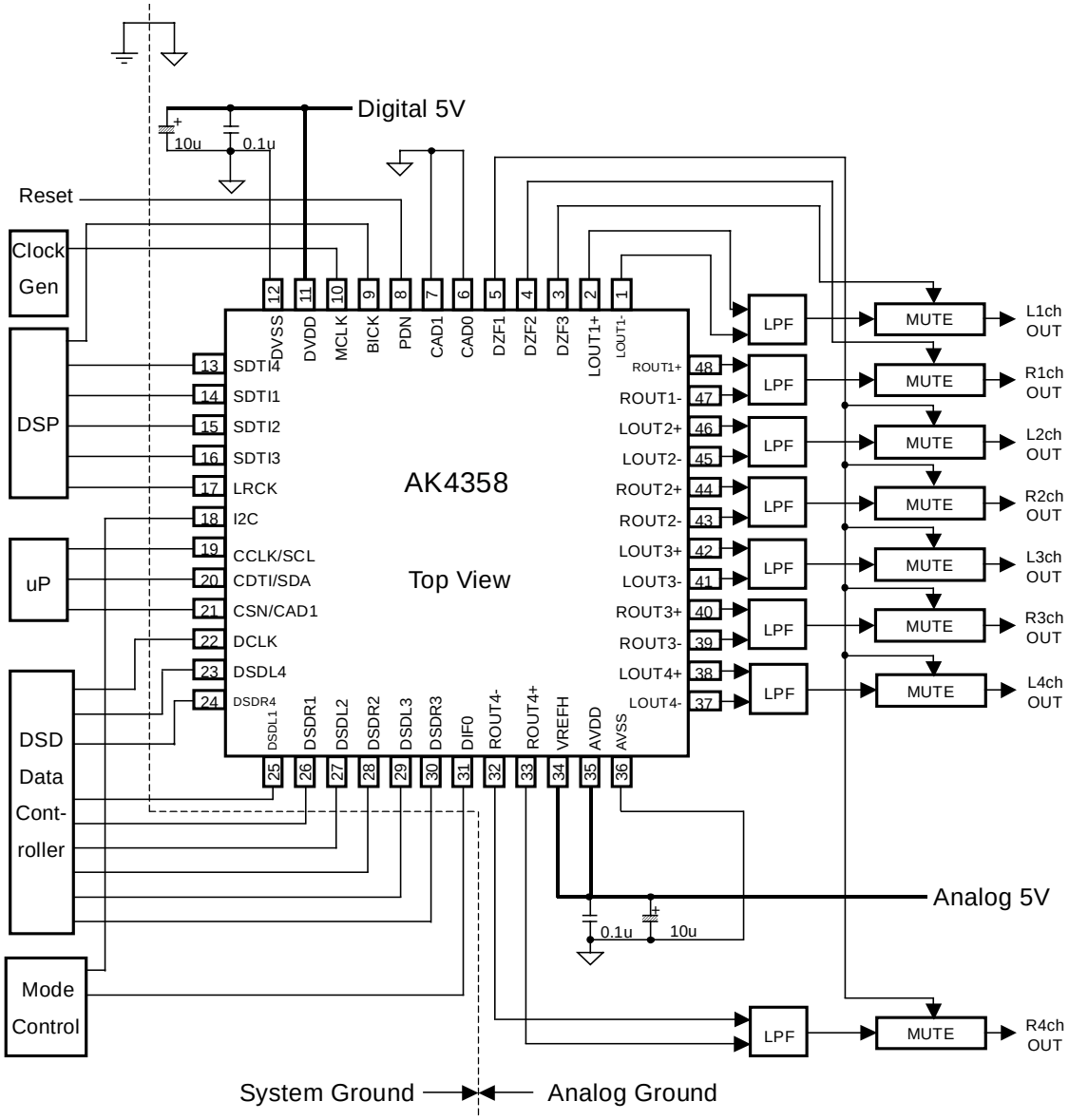


Figure 25. Typical Connection Diagram

Notes:

- LRCK = fs, BICK = 64fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down pins should not be left floating.

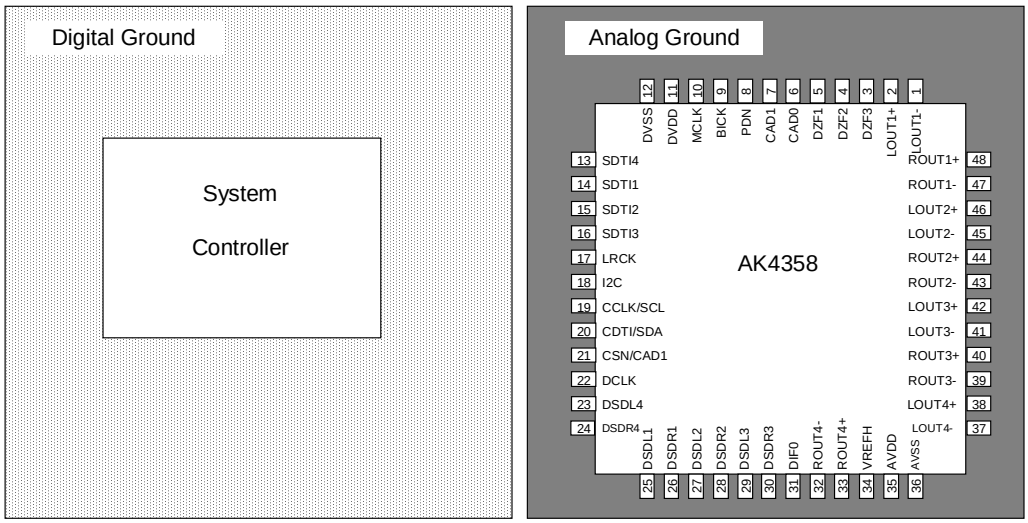


Figure 26. Ground Layout

AVSS and DVSS must be connected to the same analog ground plane.

1. Grounding and Power Supply Decoupling

AVDD and DVDD are usually supplied from analog supply in system and should be separated from system digital supply. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS and DVSS of the AK4358 must be connected to analog ground plane**. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitor, especially 0.1μF ceramic capacitor for high frequency should be placed as near to AVDD and DVDD as possible.

2. Voltage Reference

VREFH sets the analog output range. VREFH pin is normally connected to AVDD with a 0.1μF ceramic capacitor. All signals, especially clocks, should be kept away from the VREFH pin in order to avoid unwanted coupling into the AK4358.

3. Analog Outputs

The analog outputs are full-differential outputs and 0.5 x VREFH Vpp (typ) centered around the internal common voltage (about AVDD/2). The differential outputs are summed externally, V_{AOUT}=(AOUT+)-(AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 5.0Vpp (typ @VREFH=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage(V_{AOUT}) is a positive full scale for 7FFFFF (@24bit) and a negative full scale for 800000H (@24bit). The ideal V_{AOUT} is 0V for 000000H (@24bit).

The internal switched-capacitor filter and external low pass filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. DC offset on AOUT+/- is eliminated without AC coupling since the analog outputs are differential.

4. External Analog Filter

It is recommended by SACD format book (Scarlet Book) that the filter response at SACD playback is an analog low pass filter with a cut-off frequency of maximum 50kHz and a slop of minimum 30dB/Oct. The AK4358 can achieve this filter response by combination of the internal filter (Table 18) and an external filter (Figure 27).

Frequency	Gain
20kHz	-0.4dB
50kHz	-2.8dB
100kHz	-15.5dB

Table 18. Internal Filter Response at DSD mode

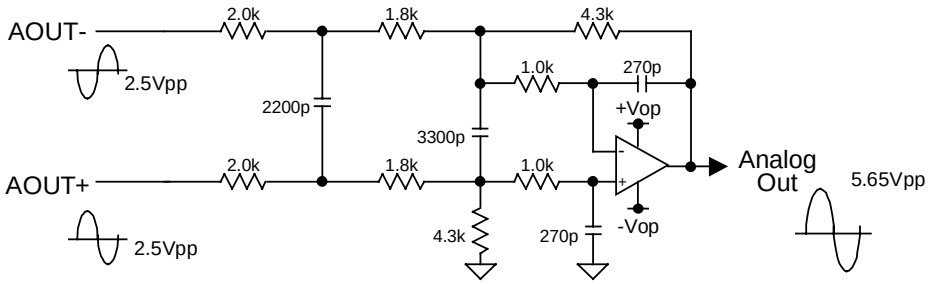


Figure 27. External 3rd order LPF Circuit Example

Frequency	Gain
20kHz	-0.05dB
50kHz	-0.51dB
100kHz	-16.8dB

DC gain = 1.07dB

Table 19. 3rd order LPF (Figure 27) Response

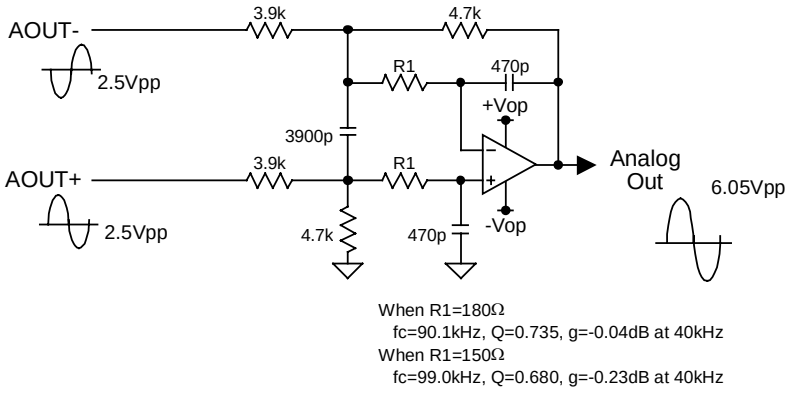
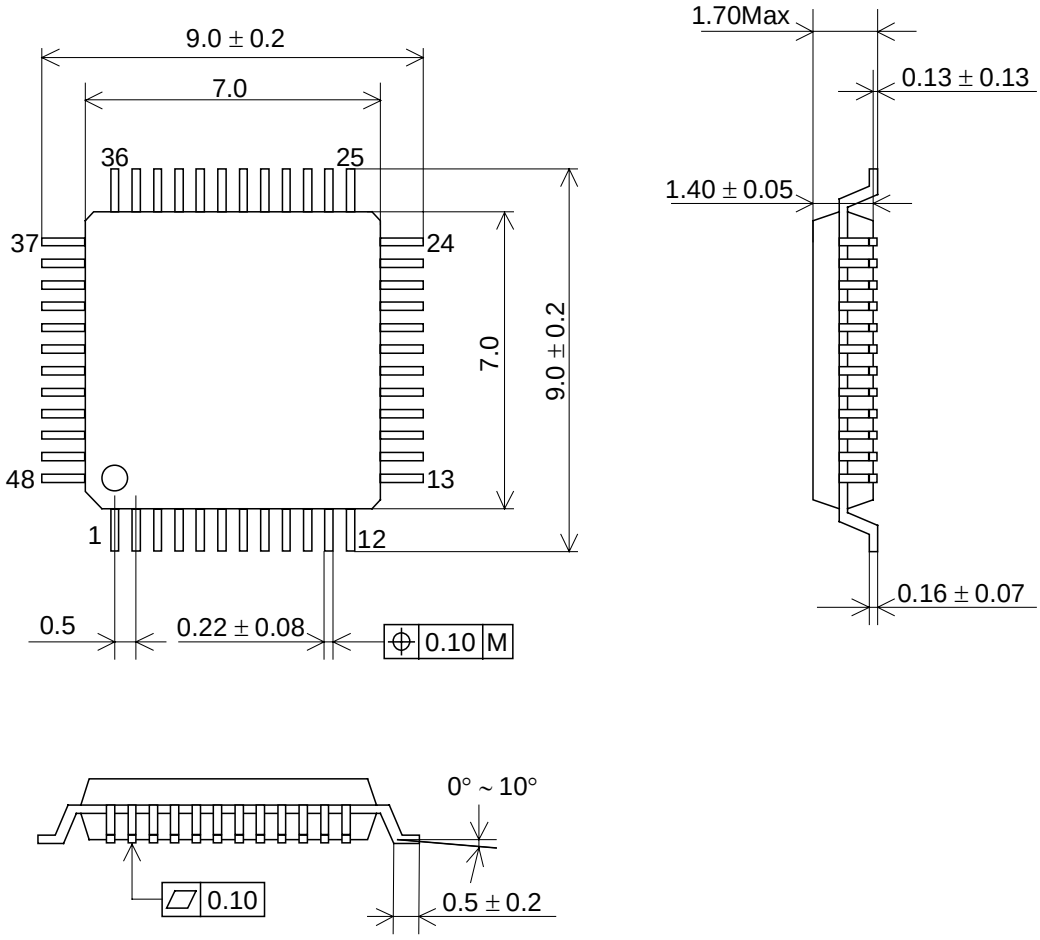


Figure 28. External 2nd order LPF Circuit Example for PCM

PACKAGE

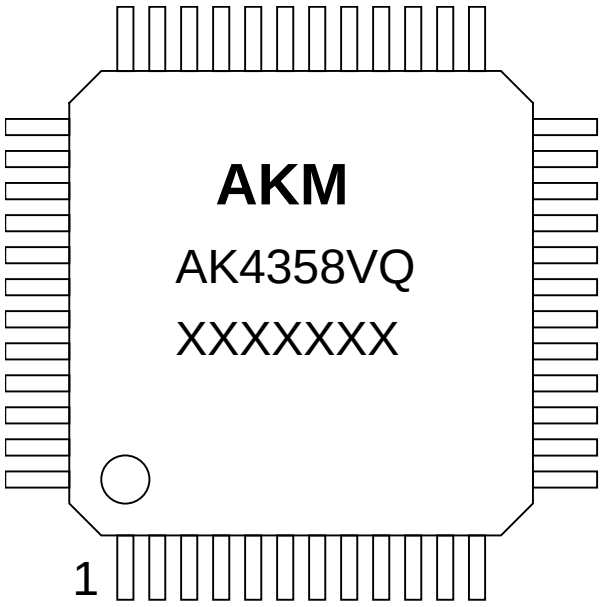
48pin LQFP(Unit:mm)



■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Asahi Kasei Logo
2) Marking Code: AK4358VQ
3) Date Code: XXXXXXX(7 digits)
4) Pin #1 indication

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
02/02/10	00	First Edition		
06/02/23	01	Spec Change	8	**SWITCHING CHARACTERISTICS** **TDM256 mode (TDM0= "H", TDM1= "L")** tLRH (min): 1/256fs → 3/256fs tLRL (min): 1/256fs → 3/256fs **TDM128 mode (TDM0= "H", TDM1= "H")** tLRH (min): 1/256fs → 3/256fs tLRL (min): 1/256fs → 3/256fs
			15	**Audio Serial Interface Format** **1) PCM Mode** "H" time and "L" time of LRCK should be 1/256fs at least. → "H" time and "L" time of LRCK should be 3/256fs at least.
			17	Figure 5,6,7 "H" time and "L" time of 3/256fs (min) was added in these timing diagrams.
			18	Figure 8,9,10 "H" time and "L" time of 3/256fs (min) was added in these timing diagrams.

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